ABSTRACT

It is aimed at improving the efficiency of data transfer processing and the concurrent data processing on a central processing unit. A data transfer device can independently request a bus access right and output an address to a first bus (IBUS) and a second bus (PBUS). It is possible to solve the state of competing for the bus access right between both buses. While the bus access right of one bus is granted for reading or writing, the bus access right of the other bus can be released. When the data transfer device releases the bus access right for the first bus, a central processing unit can process data. In response to one data transfer start request, the bus access right is requested for one bus and the other bus, There is not used a sequence of requesting the bus access right in response to different data transfer requests for respective buses. It is possible to simplify a handshake sequence of a data transfer request and its acknowledgment.